

Amendments to the Claims

1. (*Currently Amended*) An integrated circuit (~~1~~) having

[[~~-~~]] a system base chip that has basic functions for a transmitting and/or receiving system for a vehicle data bus, namely at least a system voltage supply (~~3~~), a system reset (~~3~~) and a monitoring function (~~2~~),

[[~~-~~]] an interface circuit (~~4, 5~~) that, in a self-contained fashion, runs at least parts of a data bus protocol, and in particular the LIN (Local Interconnect Network) protocol, that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte,

[[~~-~~]] a serial/parallel converter (~~2~~) that makes use in its conversion of the bit-rate detected by the interface circuit (~~4, 5~~).

2. (*Currently Amended*) An integrated circuit as claimed in claim 1, characterized in that there is provided in the integrated circuit (~~1~~) an R/C oscillator (~~6~~) that acts as a clock-signal source and as a timebase for the bit-rate detection.

3. (*Currently Amended*) An integrated circuit as claimed in claim 2, characterized in that the clock signal generated by the R/C oscillator (~~6~~) may also be provided to circuits outside the integrated circuit (~~1~~), and in particular to a microprocessor (~~7~~).

4. (*Currently Amended*) An integrated circuit as claimed in claim 1, characterized in that the interface circuit (~~4, 5~~) may also pass on complete messages.

5. (*Currently Amended*) An integrated circuit as claimed in claim 1, characterized in that the interface circuit (~~4, 5~~) performs buffer-storage of data received [[and/]] or to be transmitted.

6. (*Currently Amended*) An integrated circuit as claimed in claim 1, characterized in that the serial/parallel converter (~~5~~) converts serial data conforming to the SCI/UART (Serial Communication Interface/Universal Asynchronous Receiver Transmitter) interface standard into parallel data, or vice versa.